Design of An Integrated Parallel Processing System
with Systolic VLSI Chips*

Wen-Tsuen Chen, Jia-Shung Wang,
Chia-Cheng Liu, Shi-Jinn Horng, Chang-Biau Yang,
Ruey-Zone Huang and Bern-Cherng Liaw
Department of Computer Science
National Tsing Hua University
Hsinchu, Taiwan 30043, Republic of China

The design of a massively parallel processing system IPU (Integrated Parallel Processing Unit) is
described in this paper. It is a two-dimensional mesh-connected parallel processing array operated in an
SIMD fashion. The current version of the IPU array is implemented with 64 systolic VLSI chips, each
of which consists of 4 processing elements (PEs). Each PE consists of a 4-bit ALU, a 64*4-bit RAM,
several 4-bit registers and some multiplexers. Four PEs are implanted in a VLSI systolic chip using 2
micron CMOS technology. The IPU Department System that acts as a bridge between the host
computer and the IPU array is also designed. We provide a high-level parallel programming
environment for conveniently designing parallel programs for this IPU array. Some experimental results
show that the performance of the IPU system is more than one hundred times faster than that of the host
computer.

Keywords: multiprocessor systems, parallel processing, VLSI, SIMD, systolic arrays, parallel
programming

Received May 11, 1990; revised January 11, 1991.
Communicated by Jhing-Fa Wang.
*This research was sponsored by ERSO, Industrial Technology Research Institute, Taiwan, Republic of China.